1.4-W 50-Gbit/s InP HEMT 1:4 Demultiplexer IC with a Multi-phase Clock Architecture

Kimikazu Sano, Koichi Murata, Hiroto Kitabayashi, Suehiro Sugitani, Hirohiko Sugahara, and Takatomo Enoki

NTT Photonics Laboratories, NTT Corporation
3-1 Morinosato Wakamiya Atsugi-shi Kanagawa, Japan
e-mail: ksano@aecl.ntt.co.jp, tel: +81 46 240 2884, fax: +81 46 240 2872

Abstract — **High-speed and low-power operation of a 1:4 demultiplexer IC with a multi-phase clock (MPC) architecture is reported. The architecture features four parallel latch lines and a toggle flip-flop (TFF) that generates a four-phase clock. The IC, which was fabricated using InP HEMTs, exhibited 50-Gbit/s error-free operation with a power consumption of 1.42 W. Compared to a conventional tree-type InP HEMT 1:4 demultiplexer IC, the IC with the MPC architecture operates at the same operating speed with only one-quarter the power consumption.**

I. Introduction

In order to meet the demand for larger transmission capacity, optical communication systems based on 40-Gbit/s electrical-time-division multiplexing (ETDM) are being developed. In the systems, 4:1 multiplexer (MUX) IC and 1:4 demultiplexer (DMUX) IC, which can link a serial 40-Gbit/s signal to four parallel 10-Gbit/s ones directly, are key components. Several 4:1 MUX/1:4 DMUX IC chipsets for the 40-Gbit/s systems have been reported with SiGe HBTs [1-3], InP HBTs [4-6], and InP HEMTs [7,8], and all of them are configured with a tree-type circuit architecture that uses a series of 2:1 MUXs or 1:2 DMUXs. Although the tree-type architecture can be implemented with an ordinary differential clock, it requires a lot of circuit elements.

As for the 4:1 MUX, to reduce the number of circuit elements, we have proposed new circuit architecture called the multi-phase clock (MPC) architecture [9]. The 4:1 MUX with the MPC architecture comprises a toggle flip-flop (TFF) that generates a four-phase clock and a 4:1 series-gated selector. We fabricated a 4:1 MUX IC with the MPC architecture by using InP HEMTs and confirmed its 50-Gbit/s error-free operation with 1.71-W power consumption [9]. The power consumption was less than 1/3 that of a conventional tree-type InP HEMT 4:1 MUX IC [8] and was achieved without any reduction of operating speed.

In this paper, a 1:4 DMUX IC with the MPC architecture is described. The 1:4 DMUX with the MPC architecture consists of four parallel latch lines and the TFF generating four-phase clock. The IC was fabricated with InP HEMTs and confirmed to operate at up to 50 Gbit/s with 1.42-W power consumption. While the operating speed of up to 50 Gbit/s is the same as that of a conventional tree-type InP HEMT 1:4 DMUX IC [8], the power consumption of 1.42 W is one-quarter that of the tree-type IC.

II. Circuit Design

Figure 1 shows the circuit block diagram of the 1:4 DMUX IC with the MPC architecture. The IC includes a TFF that generates a four-phase clock, four parallel latch lines that demultiplex a 4f-(bit/s) input to four parallel f-(bit/s) out-

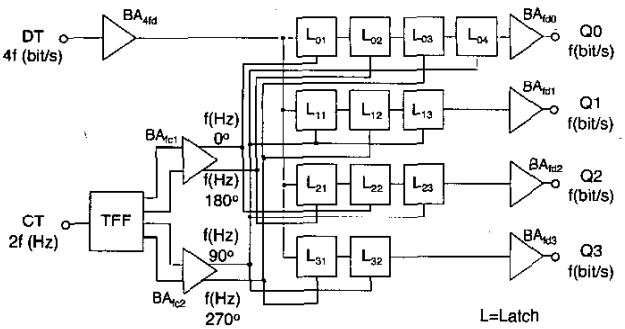

Figure 1. Circuit block diagram of the 1:4 demultiplexer IC with the multi-phase clock (MPC) architecture.

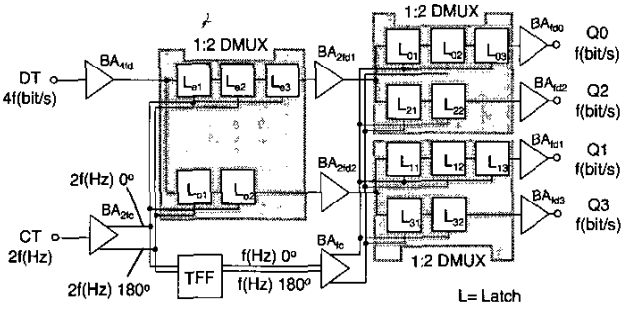

Figure 2. Circuit block diagram of a 1:4 demultiplexer IC with a conventional tree-type architecture.

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puts and deskew the outputs, and buffer amps that distribute or output signals. For a comparison, a block diagram of the 1:4 DMUX with the conventional tree-type architecture is shown in Fig. 2. The numbers of circuit elements, including buffer amps, are 20 and 25 for the MPC and the tree-type, respectively. Here, the circuit elements that the MPC eliminates are the ones that handle 2f-(bit/s) data and 2f-(Hz) clock, which consume more power than those handling f-(bit/s) data or f-(Hz) clock in order to guarantee 2f-(bit/s) or 2f-(Hz) high-speed operations. Therefore, a larger reduction of power consumption is expected with the MPC.

Figure 3 shows a circuit diagram of the latch circuit used in the MPC. It is configured with conventional source-coupled FET logic (SCFL) circuitry. The latch holds and outputs the input data taken in at the rising edge of the clock during the high-level of the clock, while it transmits and outputs the input data during the low-level. The TFF in the MPC is a master-slave type configured with two latches, and it is identical to that in the 4:1 MUX with the MPC [9]. In the master-slave type TFF, the output of the master part precedes that of the slave part by 90°. In addition, the outputs of the TFF are differential, so that the four-phase clock of 0°, 90°, 180°, and 270° is output. Buffer amps are also configured with the SCFL circuitry.

Figure 4 shows the timing chart of the 1:4 DMUX with the MPC architecture. Each of the first latches in the latch lines (L_{01}, L_{11}, L_{21}, and L_{31}) is driven by one of the four-phase clocks; that is, L_{01}, L_{11}, L_{21}, and L_{31} are driven by the 0°, 90°, 180°, and 270° clock, respectively. Each latch line thus takes in a different data stream every 4 bits. For example, the latch line for the Q0 output takes in the data stream 0A, 0B... . The second latches in the latch lines are driven by the complementary clocks for the first latches. As a result, f-(bit/s) NRZ data are outputs in the second latches. Although the 1:4 demultiplexing itself is executed only by the first and second latches, there still remains an output phase difference between latch lines as shown in Fig. 4 (L_{02} OUT, L_{12} OUT, L_{22} OUT, and Q3). To deskew and align the output phases with the 270° clock, the third or the fourth latches driven by the 270° or 90° clock are added in the latch lines for the Q0, Q1, and Q2 output. Consequently, four parallel f-(bit/s) streams aligned with the 270° clock are obtained.

III. Fabrication

The DMUX IC with the MPC architecture was fabricated on a 3-inch wafer using 0.1-μm InP HEMTs [11]. The transconductance (g_m) and current cutoff frequency (f_T) are 1.16 S/mm and 172 GHz, respectively. The threshold voltage (V_{th}) is -490 mV with a standard deviation of 20 mV.

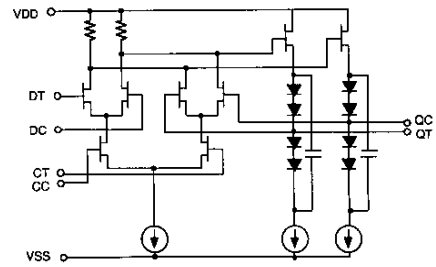


Figure 3. Circuit diagram of the latch circuit.

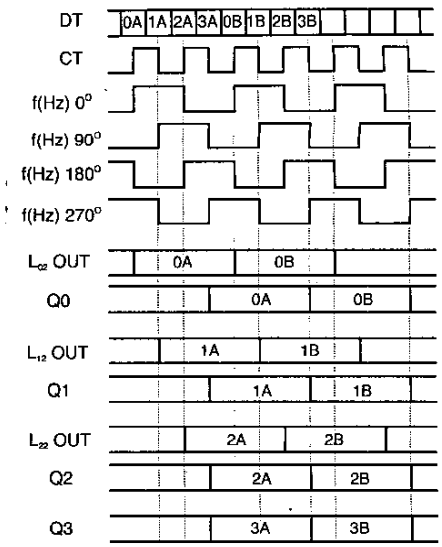
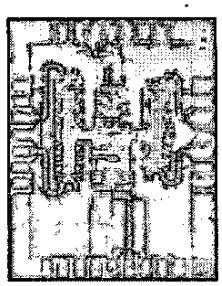


Figure 4. Timing chart of the1:4 demultiplexer IC with the MPC architecture.



Chip Size:
2.5 mmx 2.0 mm

Figure 5. Chip photograph of the 1:4 demultiplexer IC with the MPC architecture.

Figure 5 shows a chip photograph of the fabricated 1:4 demultiplexer IC. The size is 2.5 mm x 2.0 mm. The number of elements is 769, which is almost half that of the tree-type1:4 demultiplexer IC with InP HEMTs (1351) [8]. All-inputs are single-ended and terminated with 50-Ω resistors. Clock input is AC-coupled, covering above 2 GHz, and data inputs are DC-coupled. Output signals are obtained from differential buffer amps; however, complementary output ports are terminated with on-chip 50-Ω resistors due to the

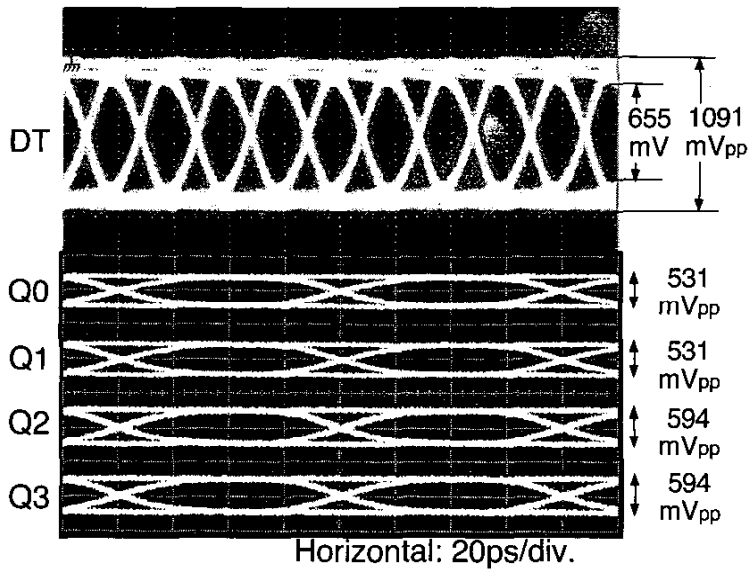


Figure 6. 50-Gbit/s operating waveforms for the 1:4 demultiplexer IC with the MPC architecture.

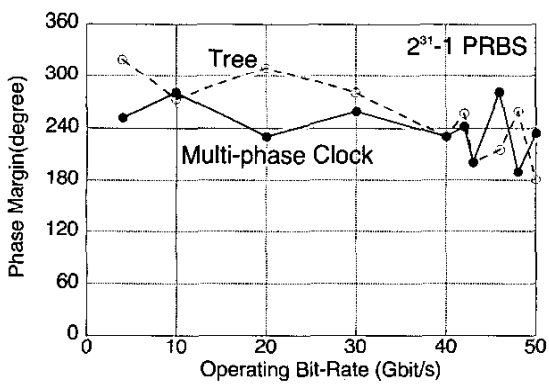


Figure 7. Operating bit-rate dependence of the phase margin of 1:4 demultiplexer ICs.
Solid: The MPC architecture.
Dotted: Conventional tree-type architecture.

Input Sensitivity

	Multi-Phase Clock (On-wafer)	Tree (Package)
43 Gbit/s	77 mV	162 mV
50 Gbit/s	235 mV	316 mV

Table 1. Input sensitivity of the 1:4 demultiplexer ICs at 43 and 50 Gbit/s.

restriction on the size of the chip.

IV. Measurement Results and Discussions

The fabricated IC with the MPC was measured on-wafer. 4f-(bit/s) PRBS data and a 2f-(Hz) clock were input. The 4f-(bit/s) data were generated by the combination of the 4-channel PPG, a 4:2 MUX, and an InP HEMT 2:1 MUX. The 2f-(Hz) clock was fed from a synthesizer that output a sinusoidal wave. The operating bit-rate range that could be tested was from 0.4 to 50 Gbit/s, which was limited by the operating range of the PPG. The amplitudes of the input data and clock were 1 Vpp, unless otherwise indicated.

Figure 6 shows the 50-Gbit/s operating waveforms of the IC. The IC operated error-free for 2^{31}-1 PRBS, where error-free means that all four parallel outputs are error-free simultaneously and the quarter-PRBS-phase shift between adjacent channels is maintained. The phase margin for the error-free operation was 234° (13 ps). The skew of the four parallel outputs at the IC output was below ±10 ps, which confirms that the output deskew function of the IC operates well. The power consumption was 1.42 W at a supply voltage of -3.3 V, which is one-quarter that of the conventional tree-type InP HEMT 1:4 DMUX IC [8]. This drastic reduction is due to the MPC architecture itself and the reduction of supply voltage from -4.5 V to -3.3 V. Furthermore, the error-

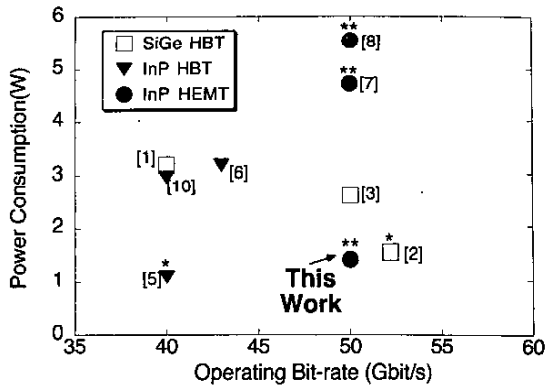


Figure 8. Power consumption and operating bit-rate of reported 40-Gbit/s-class 1:4 demultiplexer ICs.

free operation was confirmed at the supply voltage from -3.0 V to -3.8 V. In this supply voltage range, the power consumption varied from 1.11 W (-3.0 V) to 1.86 W (-3.8 V).

The IC was also tested at a wide range of operating bit-rates. Figure 7 shows the operating bit-rate dependence of the phase margin for the MPC. For comparison, the dependence for the tree-type IC [8] is also plotted. From 4 to 50 Gbit/s, a phase margin of more than 180° was confirmed for both architectures. In spite of its lower power consumption, the MPC does not sacrifice the phase margin, even in high-speed operation.

We also measured the input sensitivity of the IC. Table 1 shows the input sensitivity of the MPC at 43 and 50 Gbit/s. Also here, the sensitivity of the tree-type InP HEMT 1:4 DMUX IC [8] is shown. The degradation of the input sensitivity due to packaging for the tree-type IC has to be taken into consideration; nonetheless, the input sensitivity of the MPC seems to be comparable or superior to that of the tree-type. This implies that the buffer amp for the input data in the MPC well amplifies and distributes the data to four parallel latch lines.

Figure 8 summarizes the power consumption and the operating bit-rate among reported 1:4 DMUX ICs for 40-Gbit/s applications, including this work. All of the reported InP HEMT ICs achieve > 50-Gbit/s operation and have led in the operating speed. On the other hand, the InP HEMT ICs consume more power than ICs based on SiGe HBTs or InP HBTs. However, this work demonstrates that the power consumption of InP HEMT ICs can be reduced to a level as low as or lower than that of SiGe HBTs and InP HBTs without sacrificing operating speed.

V. Conclusion

An InP HEMT 1:4 DMUX IC with an MPC architecture has been described. It features four parallel latch lines and a TFF that generates four-phase clock. The fabricated IC operated error free for 2^{31}-1 PRBS from 4 to 50 Gbit/s with a phase margin of > 180°. The power consumption was 1.42 W at a supply voltage of -3.3 V. Compared with the conventional tree-type InP HEMT 1:4 DMUX IC, the MPC IC operates with one-quarter the power consumption while maintaining the operating speed and the phase margin.

Acknowledgment

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